Docket No.: 043876-0145 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Craig HANSEN et al.	:	Confirmation Number: 3618
Application No.: 10/646,787	:	Group Art Unit: 2181
Filed: August 25, 2003	:	Examiner: Henry TSAI

For: PROGRAMMABLE PROCESSOR WITH GROUP FLOATING-POINT OPERATIONS

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

These Comments on Statement of Reasons for Allowance are filed in response to the Notice of Allowability mailed on June 2, 2006.

Applicants respectfully traverse the Examiner's Statement on Reasons for Allowance. Entry of that Statement into the record should not be construed as any agreement with or acquiescence by Applicants in the stated reasoning.

Applicants note that claim 1 recites:

1. A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and

a multi-precision execution unit coupled to the data path, the multi-precision execution unit configurable to dynamically partition data received from the data path to account for an elemental width of the data wherein the elemental width of the data is equal to or narrower than the data path, the multi-precision execution unit being capable of performing group floating-point operations on multiple operands in partitioned fields of operand registers and returning catenated results.

Applicants note that claim 35 recites:

35. A data processing system, comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable processor coupled to the bus, the programmable processor comprising:

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and

an execution unit, coupled to the instruction path and data path, operable to decode and execute instructions received from the instruction path wherein, in response to decoding a single instruction specifying an elemental width of operands and a floating-point arithmetic operation, the execution unit

(i) partitions data received from the data path and stored in an operand register based on the elemental width specified in the instruction into a plurality of operands stored in partitioned fields of the operand register,

(ii) performs the floating-point arithmetic operation on each of the plurality of operands to produce a plurality of individual results, and

(iii) returns the plurality of individual results to a register as a catenated result, where each of the plurality of operands operated on by the floating-point arithmetic operation and each of the plurality of individual results returned by the floating-point arithmetic operation comprise floating-point data having a sign bit, an exponent, and a mantissa, and wherein

the execution unit is capable of decoding and executing a plurality of different data handling instructions, each data handling instruction specifying a data handling operation to be applied individually and separately to each of a plurality of operands stored in partitioned fields of an operand register to return a catenated result to a register, where each of the plurality of operands operated on by the data handling operation comprises integer data and the catenated result returned by the data handling operation comprises a plurality of partitioned fields storing integer data.

Applicants note that claim 42 recites:

42. A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable microprocessor, coupled to the bus, capable of operation independent of another host processor, the programmable microprocessor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path,

a cache operable to retain data communicated between the external interface and the data path,

at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path, and

an execution unit, coupled to the instruction path and data path, operable to decode and execute instructions received from the instruction path, wherein the execution unit is configurable to partition data, on an instruction-by-instruction basis, stored in an operand register having a width of n bits into a plurality of operands, each operand having an elemental width of m contiguous bits such that m times the number of operands equals n, the execution unit being capable of executing group floating-point arithmetic instructions that perform a floating-point operation on each of the plurality of operands to produce a plurality of individual m-bit results that are returned to a register in the register file as a catenated result, wherein the elemental width of the partitioned data is determined by the instruction and wherein the floating-point data comprises a sign bit, an exponent, and a mantissa.

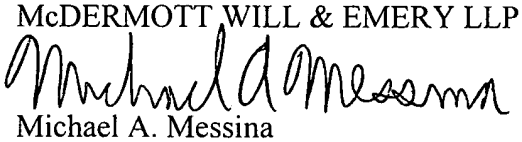
None of the prior art references teaches or suggests a system as recited in any of these claims.

It is respectfully submitted that the allowed claims should be entitled the broadest reasonable interpretation and broadest range of equivalents that are appropriate in light of the language of the claims, the supporting disclosure and Applicants' prosecution of the claims, without reference to the Statement of Reasons for Allowance.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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